Improved the two DC capacitors' voltage balancing of three-level NPC inverters applied in electric vehicles

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Abstract:

Excessive unbalance of the DC capacitor voltages of the inverter can cause overvoltages on power components and capacitors, causing unintended low-order harmonics on the load side such as second harmonics, 3rd, 4th, 5th, ..., causing direct harm to the motor load, reducing the controllability of the reverse voltage and filter compensating current for the active filter circuit, affect to the performance of electric vehicles (EVs). Therefore, maintaining the DC capacitors' voltage balance will control the multi-level inverter's input quality and ensure the output quality in terms of Total Harmonic Distortion (THD). The paper proposes a method to control the two DC capacitors' voltage balance of the 3-level inverter, using the principle of offset function separation. The analysis results suggest that the NPC three-level modulation technique should be implemented to satisfactorily achieve the neutral line current (*iNP*). Compared with recent international publications, the proposed new algorithm can save and reduce switching loss; the transient dynamic response can be adjusted easily. Maintaining the capacitor voltage balance allows the design with the smallest capacity to reduce voltage stress on components. The proposed results are partially verified through simulation and experiment.

Keywords: Electric vehicle; AFS; Steering system; Braking system; ABS; Battery management systems; BMS; Inverter.

1. Introduction

Electric vehicles (EVs) are based on electric powertrains powered by electric motors without the use of internal combustion engines. All power is derived from electrical energy [1], [2]. The main advantage is high efficiency of energy conversion through the electric motor system. Recently, there has been a lot of research and development in both academic and industrial sectors. Commercial electric vehicles are already available and gaining an increasingly large market share worldwide [3]. Many countries incentivize users through lower taxes or exemptions, free parking, and free electric vehicle charging stations.

On the other hand, hybrid electric vehicles (HEVs) are evidence of a gradual transition, a stepping stone towards a complete shift from gasoline-powered to electric vehicles [4]. They have been used widely for several decades. Virtually all car manufacturers have at least one hybrid electric vehicle model. With the European Union's decision to stop selling fossil-fuel-powered cars by 2035, electric vehicles (EVs) will undoubtedly dominate the future market. The strong development of electric vehicles lies in the powertrain technology of the systems within electric cars [5], [6], [7], as shown in Figure 1.

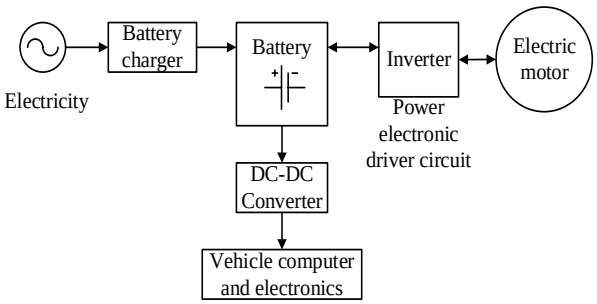


Figure 1. The main components of an electric vehicle.

The battery served as the primary energy storage unit. A battery charger converts electricity from a

power source to charge the battery [8], [9], [10]. The DC voltage of the battery was converted (inverted) into an AC voltage to control the electric motor [11]. Other components in the vehicle can be supplied with DC power from the battery through a DC-DC converter to reduce the voltage from the battery's DC source to lower voltages, such as 5V-20V.

This research focuses on improving inverters [12] in electric vehicles. Using a new technique involving the balancing of the DC-link voltage in a 3-level NPC inverter to control the input quality of the multi-level NPC inverter and ensure the output quality in terms of Total Harmonic Distortion (THD) [13] enhances the operational efficiency of the electric motor [14].

2. Analyzing the current waveform in a three-level neutral-point-clamped (NPC) inverter using a two-level technique

The control of neutral current (neutral-point-clamped (NPC)), as shown in Figure 2, in multilevel inverters is one of the most critical tasks of modulators [14]. Balancing the neutral-point potential (NPP) depends on the current injected into the neutral point (NP).

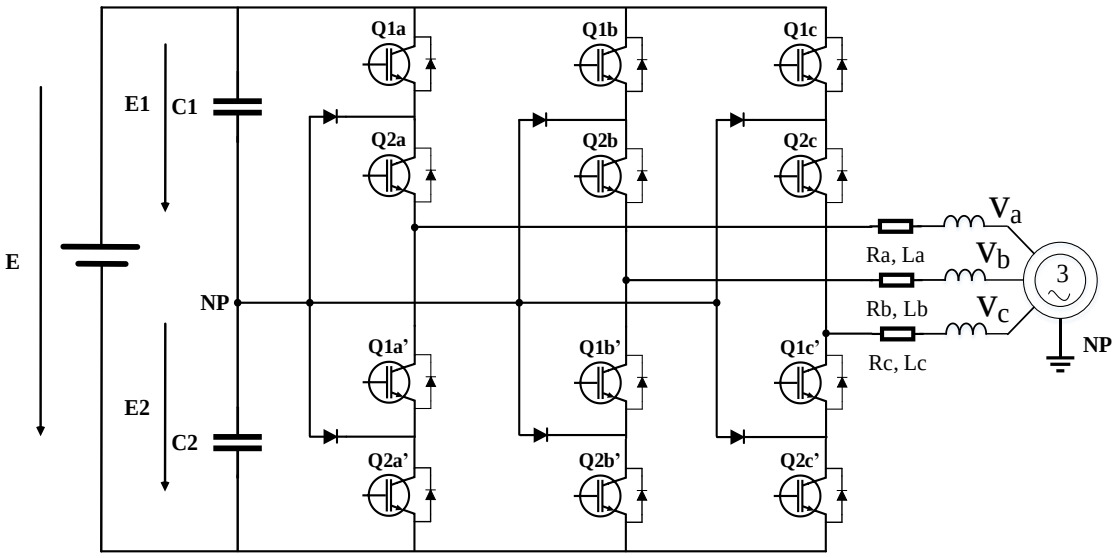


Figure 2. A schematic diagram of the 3-level voltage source inverter circuit.

This current is a result of the modulation process and phase-current components, which may include harmonic or DC components. The currents generate ripples in the NP potential with an amplitude that can be determined by the capacitance function of the link capacitors (Cdc link). However, the DC component causes an imbalance in the NPP [13], [15].

The definitions of max, mid, and min are the fundamental voltage values of the three phases arranged in descending order, calculated in units, with the corresponding phase currents as i_max, i_mid, and i_min. The addition of the voltage offset v_0 to the fundamental voltage results in a three-phase inverter voltage. The average inverter voltage was adjusted by changing the output voltage levels between 0, 1, and 2.

$$\text{max} + \text{mid} + \text{min} = 0 \quad (1)$$

$$\text{i\_max} + \text{i\_mid} + \text{i\_min} = 0 \quad (2)$$

Where:

$$\text{max} = max(v_{a(1)}, v_{b(1)}, v_{c(1)})$$

$$\text{min} = min(v_{a(1)}, v_{b(1)}, v_{c(1)})$$

$$mid = -\text{max} - \text{min}$$

The 2-level modulation technique in the multilevel inverter is implemented so that the instantaneous voltage switches between the two nearest voltage levels in each sampling cycle. If the control voltages for the three phases are given as $v\_{a0} = 1.8$, $v\_{b0} = 1.5$, and $v\_{c0} = 0.4$, then phases A and B switch between 1 and 2, whereas phase C switches between 0 and 1. By combining the switching possibilities of phases A, B, and C between levels (1;2), (1;2), and (0;1), it creates the voltage vector diagram of the virtual 2-level inverter centered at [1,1,0]. Let v_{0} be the auxiliary offset voltage added to the fundamental

inverter voltage. With the virtual 2-level inverter centered at [1,1,0], the following relationship holds:

$$1 \le v'_{a0} \le 2; 1 \le v'_{b0} \le 2; 0 \le v'_{a0} \le 1 \qquad (3)$$

Consider the 2-level modulation technique in sector 1 of the hexagonal space vector diagram shown in Figure 3. In sector 1, phase A has the highest average voltage value (max), phase C has the lowest (min), and phase B has an intermediate average value (mid). Sector 1 can be further divided into four regions: (1) to (4).

In region (1), the 2-level modulation technique can be applied with one of the four virtual 2-level inverter voltages, each with its corresponding center located at positions [0,0,0], [1,1,1], [1,0,0], and [1,1,0]. For region (2), it is possible to apply the 2-level technique to one of the two virtual 2-level inverter voltages, with centers at [1,0,0] and [1,1,0].

In regions (2) and (4), only the 2-level modulation technique can be applied to one virtual 2-level inverter voltage, with coordinates [1,0,0] for the region (2) and [1,1,0] for the region (4).

If a predefined offset function is given, the DC input current into the neutral point can be controlled through the local offset function value ξ_0. Therefore, it is possible to establish the current function i_{NP} depending on the local offset function. In the cases being examined, to simplify matters, the format of the offset function is chosen such that the current $i_{NP} = i_{NP1}$ corresponds to the value $\xi_0 = 0$, and the current is achieved when $\xi_0 = \xi_{\max}$.

Zone (1): The following condition is satisfied: (max-min) < 1. Considering 4 cases following:

(1a) Virtual 2-level inverter with the center vector at [0,0,0], offset function format: $v_0 = -\min$. Local offset limit:

$$\xi_{0\min} = 0; \xi_{0\max} = 1 - \max + \min \qquad (4)$$

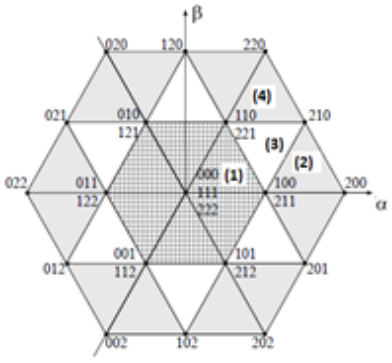


Figure 3. Voltage vector diagram of the 3-level NPC inverter and the division of triangular regions.

The positions of the three inverter voltages corresponding to a local offset of 0 are shown in Figure 2. The current i_{NP} does not change when shifted, and is controlled by the effect of the local offset:

$$i_{NP} = i_{NP1} = \max.i_{\max} + mid.i_{mid} + \min.i_{\min} \qquad (5)$$

(1b) The 2-level inverter with a center vector at [1,0,0] with an offset format: $v_0 = 1 - \max$. The local offset limits are:

$$\xi_{0\min} = 0; \xi_{0\max} = \max - mid \qquad (6)$$

The current i_{NP} with a local offset of zero is:

$$i_{NP1} = \max.i_{\max} + mid.i_{mid} + \min.i_{\min} \qquad (7)$$

The *current* function i_{NP} with respect to the local offset ξ_0 is expressed as:

$$\begin{aligned} & i_{NP} = \max.i_{\max} + mid.i_{mid} + \min.i_{\min} \\ & -2\xi_0 i_{\max} = i_{NP1} - 2\xi_0 i_{\max} \end{aligned} \qquad (8)$$

The value of *the* current i_{NP} when the local offset reaches an extremum is:

$$\begin{aligned} & i_{NP2} = \max.i_{\max} + mid.i_{mid} + \min.i_{\min} - \\ & -2(\max - mid)i_{\max} = (-\max + mid).i_{\max} \\ & +(\min - mid).i_{\min} \end{aligned} \qquad (9)$$

(1c) The 2-level inverter with a center at [1,1,0] with an offset function format: $v_0 = 1 - mid$. The local offset limits were determined as follows:

$$\Rightarrow \quad \xi_{0\min} = 0; \xi_{0\max} = mid - \min \qquad (10)$$

The current function i_{NP} with respect to the local offset and its extremum values are as follows:

$$i_{NP} = (-\max + mid).i_{\max} + (\min - mid).i_{\min} + 2\xi_0 i_{\min} = i_{NP1} + 2\xi_0 i_{\min} \quad (11)$$

$$i_{NP1} = (-\max + mid).i_{\max} + (\min - mid).i_{\min} \quad (12)$$

$$i_{NP2} = -\max.i_{\max} - mid.i_{mid} - \min.i_{\min} \quad (13)$$

(1d) The 2-level inverter with a center vector at [1,1,1] with an offset function format: $v_0 = 1 - \min$, and the local offset limits:

$$\xi_{0\min} = 0; \xi_{0\max} = 2 - \max + \min \quad (14)$$

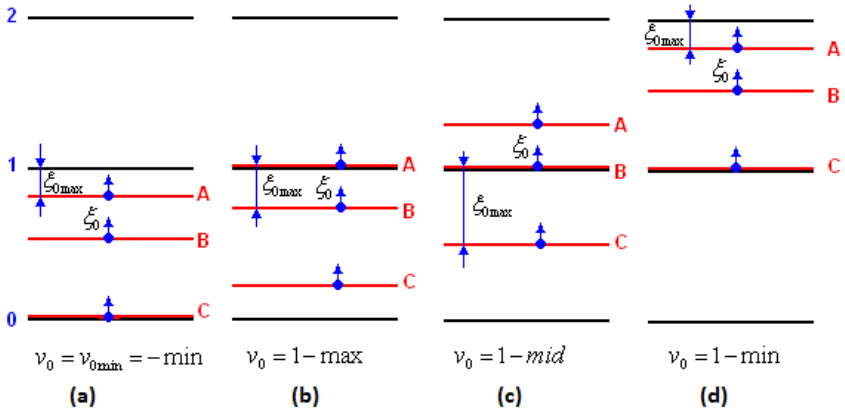


Figure 4. The quantities A, B, and C correspond to the max, mid, and min phase signals within the region (1).

The current i_{NP} remained unchanged when the local offset was altered:

$$i_{NP} = i_{NP1} = -\max.i_{\max} - mid.i_{mid} - \min.i_{\min} \quad (15)$$

From the analysis results, we can observe the following: (a) within region (1), only cases (1b) and (1c) affect the current i_{NP} through the local offset, and (b) one extremum i_{NP} of (1b) always has the opposite sign of one extremum of (1c), allowing control of any signed current i_{NP} in region (1). As a result, the 2-level PWM control technique can always be applied to the region (1) to achieve capacitor balancing [16].

Region (2): Satisfying the following conditions (max-min) > 1, (max-mid) > 1, and (mid-min) <1. The offset function format is $v_0 = -\min$, with the vector diagram centered at [1,0,0]. The inverter voltages are located at positions in Figure 4:

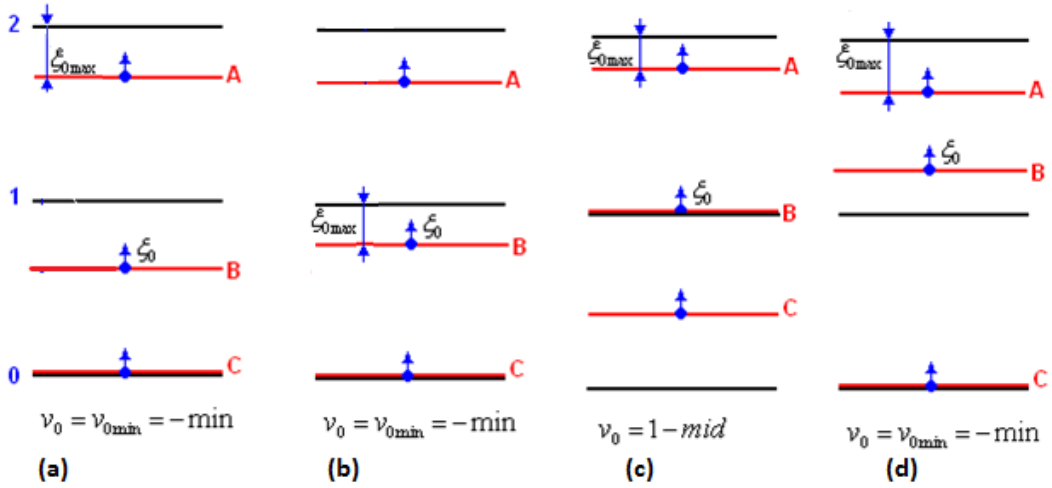
$$\xi_{0\min} = 0; \xi_{0\max} = 2 - \max + \min \quad (16)$$

The current function i_{NP} and its extremum values are:

$$i_{NP} = (2 - \max + \min - \xi_0)i_{\max} + (mid - \min + \xi_0)i_{mid} + \xi_0 i_{\min} \quad (17)$$

$$i_{NP} = i_{NP1} - 2\xi_0 i_{\max} \quad (18)$$

$$i_{NP1} = (2 - \max + \min)i_{\max} + (mid - \min)i_{mid} \quad (19)$$



Figurer 5. The max, mid, and min phase quantities in regions (2) - case (a), (3) - cases (b) and (c), and (4) - case (d).

$$i_{NP2} = (2 - \max + \min) i_{\max} + (mid - \min) i_{mid} - 2(2 - \max + \min) i_{\max} \quad (20)$$

$$i_{NP2} = \max . i_{\max} + mid . i_{mid} + \min . i_{\min} - 2 i_{\max} \quad (21)$$

Region (3): Satisfying the conditions (max-min) > 1, (max-mid) < 1, and (mid-min) < 1. Two cases can occur in this region, as shown in Figures 4 and 5.

(3a) Center vector at [1,0,0]: $v_0 = -\min$

$$\xi_{0\min} = 0; \xi_{0\max} = 1 - mid + \min \quad (22)$$

The current function i_{NP} and its extremum values are:

$$i_{NP} = (2 - \max + \min - \xi_0) i_{\max} + (mid - \min + \xi_0) i_{mid} + \xi_0 i_{\min} \quad (23)$$

$$i_{NP} = i_{NP1} - 2\xi_0 i_{\max} \quad (24)$$

$$i_{NP1} = (2 - \max + \min) i_{\max} + (mid - \min) i_{mid} \quad (25)$$

$$i_{NP2} = (2 - \max + \min) i_{\max} + (mid - \min) i_{mid} - 2(1 - mid + \min) i_{\max} \quad (26)$$

$$i_{NP2} = 3.mid . i_{\max} + (mid - \min) i_{mid} \quad (27)$$

(3b) Center vector at [1,1,0]: $v_0 = 1 - mid$

$$\xi_{0\min} = 0; \xi_{0\max} = 1 - \max + mid \quad (28)$$

The current function i_{NP} and its extremum values are:

$$i_{NP} = i_{NP1} + 2\xi_0 i_{\min} \quad (29)$$

$$i_{NP1} = 3.mid . i_{\max} + (mid - \min) i_{mid} \quad (30)$$

$$i_{NP2} = (-\max + mid) . i_{\max} + (2 - 3\max) i_{\min} \quad (31)$$

Region (4): Satisfying the conditions (max-min) > 1; (max-mid) < 1, and (mid-min) > 1.

By setting $v_0 = -mid$, a 2-level switching occurs with a virtual 2-level inverter centered at vector [1,1,0]. The three inverter phases formed have relative positions, as shown in Figure 5. The local offset limits are:

$$\xi_{0\min} = 0; \xi_{0\max} = 2 - \max + \min \quad (32)$$

The current function i_{NP} and its extremum values are:

$$i_{NP} = (2 - \max + \min - \xi_0) i_{\max} + (2 - mid + \min - \xi_0) i_{mid} + \xi_0 i_{\min} \quad (33)$$

$$i_{NP} = i_{NP1} + 2\xi_0 i_{\max} \quad (34)$$

$$i_{NP1} = (2 - \max + \min) i_{\max} + (2 - mid + \min) i_{mid} = -\max . i_{\max} - mid . i_{mid} - \min . i_{\min} - 2 i_{\min} \quad (35)$$

$$i_{NP2} = (2 - \max + \min) i_{\max} + (2 - mid + \min) i_{mid} + 2(2 - \max + \min) i_{\min} \quad (36)$$

$$i_{NP2} = -\max . i_{\max} - mid . i_{mid} + \min . i_{\min} - 2\max . i_{\min} + 2 i_{\min} \quad (37)$$

Control of DC Capacitor Voltage Balancing: The reference current i_{NP}^* is defined as the output of the DC capacitor voltage-balancing controller. In the ideal case, $i_{NP}^* = 0$.

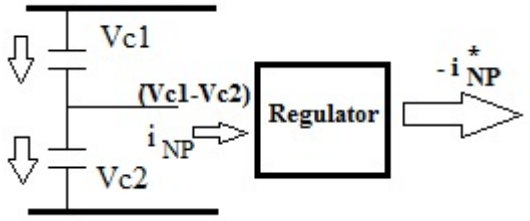


Figure 6. Principle for controlling the voltage difference between two DC capacitors.

Simple Controller: The local offset function i_{NP}^* can be established depending on the demand current as follows:

$$\xi_0 = \begin{cases} \dfrac{i_{NP}^* - i_{NP1}}{-2 i_{\max}} & for \begin{cases} Min(i_{NP1}, i_{NP2}) < i_{NP}^* \\ i_{NP}^* < Max(i_{NP1}, i_{NP2}) \end{cases} \\ \xi_{0\max} & for \begin{cases} \begin{cases} (Min(i_{NP1}, i_{NP2}) > i_{NP}^*) \\ (i_{NP1} > i_{NP2}) \end{cases} \\ \begin{cases} (Max(i_{NP1}, i_{NP2}) < i_{NP}^*) \\ (i_{NP1} < i_{NP2}) \end{cases} \end{cases} \\ 0 & for \quad else \end{cases} \quad (38)$$

Or:

$$\xi_0 = \begin{cases} \dfrac{i_{NP}^* - i_{NP1}}{2 i_{\min}} & for \begin{cases} Min(i_{NP1}, i_{NP2}) < i_{NP}^* \\ i_{NP}^* < Max(i_{NP1}, i_{NP2}) \end{cases} \\ \xi_{0\max} & for \begin{cases} \begin{cases} (Min(i_{NP1}, i_{NP2}) > i_{NP}^*) \\ (i_{NP1} > i_{NP2}) \end{cases} \\ \begin{cases} (Max(i_{NP1}, i_{NP2}) < i_{NP}^*) \\ (i_{NP1} < i_{NP2}) \end{cases} \end{cases} \\ 0 & for \quad else \end{cases} \quad (39)$$

The characteristic of the capacitor balancing control technique when setting the local offset function using extremum values is a discontinuous modulation mode, allowing for reduced switching losses.

3. Analysis of DC neutral current in 3-level modulation technique

Unlike the case of the 2-level modulation technique, the 3-level modulation technique allows the DC neutral current to have any direction, thus providing a convenient means for balancing the DC capacitors[6], [17].

The inverter voltage, for example, phase A, can sequentially switch between voltage levels 0, 1, and 2 over the corresponding time periods denoted as d_{0A}, d_{1A}, and d_{2A}. A 3-level modulation pattern with reduced switching events is shown in Figure 5. The phase with the highest voltage-max, and the phase with the lowest voltage-min, can be modulated in a 2-level fashion. The remaining phase-mid, will perform 3-level switching. The time at which the phase-max is maintained at levels 2 and 1 are denoted as d_{1max} and d_{2max}, respectively.

3.1. In the case where the current i_{NP} is equal to zero

The 3-level modulation pattern in Figure 7 is designed to achieve zero DC neutral current. To achieve this, the total offset function is set as:

$$v_0^{'} = v_0 + \xi_0 = 1 - (\max + \min)/2 \qquad (40)$$

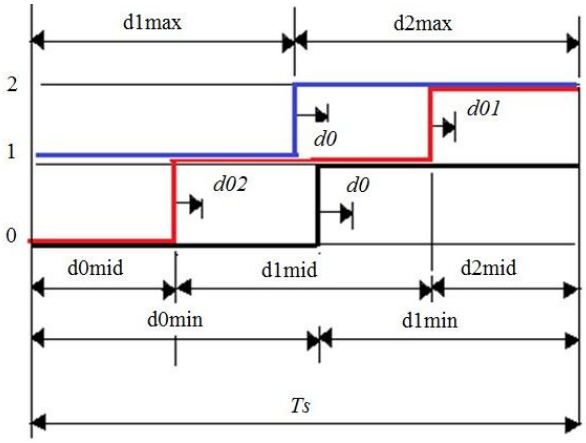


Figure 7. Illustration of the switching pattern in the 3-level modulation technique for 3-level NPC inverter.

As a result, the voltages across the inverter branches are equal to:

$$\begin{aligned} \max 0 &= 1 + (\max - \min)/2 \\ mid\,0 &= 1 - 3(\max + \min)/2 \\ \min 0 &= 1 - (\max - \min)/2 \end{aligned} \qquad (41)$$

The condition for i_{NP} to be equal to zero is as follows:

$$d_{1\max} i_{\max} + d_{1mid} i_{mid} + d_{1\min} i_{\min} = 0 \qquad (42)$$

Solving for this yields equation (43):

$$\begin{aligned} d_{2\max} &= (\max - \min)/2; \\ d_{1\max} &= 1 - (\max - \min)/2; \\ d_{2mid} &= (mid - \min)/2; \\ d_{1mid} &= 1 - (\max - \min)/2; \\ d_{0mid} &= (\max - mid)/2; \\ d_{1\min} &= 1 - (\max - \min)/2; \\ d_{1\min} &= 1 - (\max - \min)/2; \\ d_{10mid} &= d_{0mid} + d_{1mid} = \\ &= 1 - (mid - \min)/2. \end{aligned} \qquad (43)$$

Note: $d_{1\max} < d_{10mid}$ and $d_{0mid} < d_{0\min}$. This result depends on the relationship between the switching times of each phase voltage at each voltage level in the switching sequence in the following cases:

$$\begin{aligned} &(i_1)\, d_{1\max} > d_{0mid} \Rightarrow \max < 2/3 \\ &(or\ d_{1\max} < d_{0mid} \Rightarrow \max > 2/3) \end{aligned} \qquad (44)$$

$$\begin{aligned} &(i_2)\, d_{1\max} > d_{0mid} \Rightarrow (\max - \min) < 1 \\ &(or\ d_{1\max} < d_{0mid} \Rightarrow (\max - \min) > 1) \end{aligned} \qquad (45)$$

$$\begin{aligned} &(i_3)\, d_{10mid} > d_{0\min} \Rightarrow \min > -\frac{2}{3} \\ &(or\ d_{10mid} < d_{0\min} \Rightarrow \min < -\frac{2}{3}) \end{aligned} \qquad (46)$$

Combining conditions (i1), (i2), and (i3), we deduce the following 5 sample 3-level modulation patterns with the corresponding graphs in Figure 6 and the area where the demand vector appears in the first sector in Figure 8:

a) $d_{1\max} < d_{0mid} < d_{10mid} < d_{0\min}$

$$\Rightarrow \begin{cases} max - min > 1 \\ max < 2/3 \\ min < -2/3 \end{cases}$$

b) $d_{1\max} < d_{0mid} < d_{0\min} < d_{10mid}$

$$\Rightarrow \begin{cases} max - min > 1 \\ max < 2/3 \\ min > -2/3 \end{cases}$$

c) $d_{0mid} < d_{1\max} < d_{10mid} < d_{0\min}$

$$\Rightarrow \begin{cases} max - min > 1 \\ max > 2/3 \\ min < -2/3 \end{cases}$$

d) $d_{0mid} < d_{1\max} < d_{0\min} < d_{10mid}$

$$\Rightarrow \begin{cases} max - min > 1 \\ max > 2/3 \\ min > -2/3 \end{cases}$$

e) $d_{0mid} < d_{0\min} < d_{1\max} < d_{10mid}$

=> (max-min) < 1

Cases with i_{NP} non-zero current:

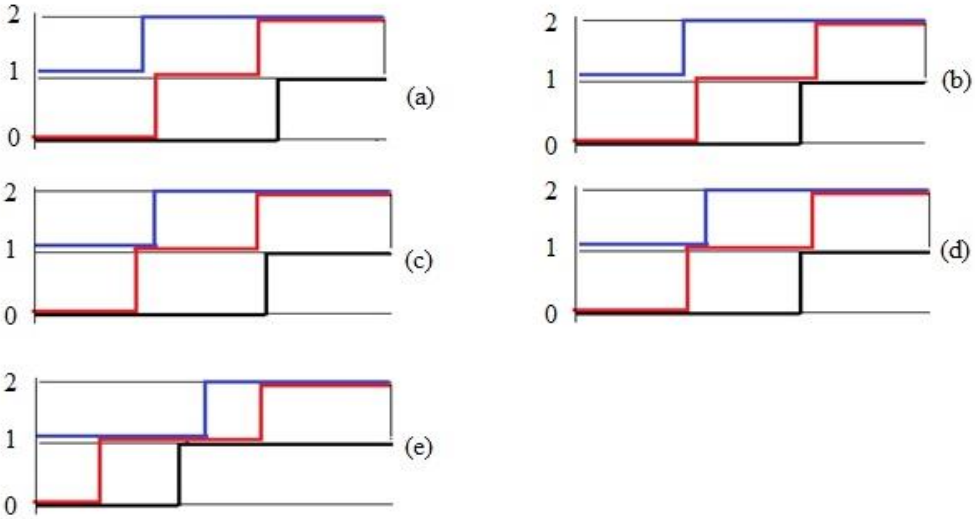


Figure 8. Five cases of current suppression mode for the 3-level NPC inverter using the 3-level switching technique.

Switching state sequence with zero NP neutral current. For example, the switching state sequence corresponding to Figure 8a is 100 → 200 → 210 → 220 → 221.

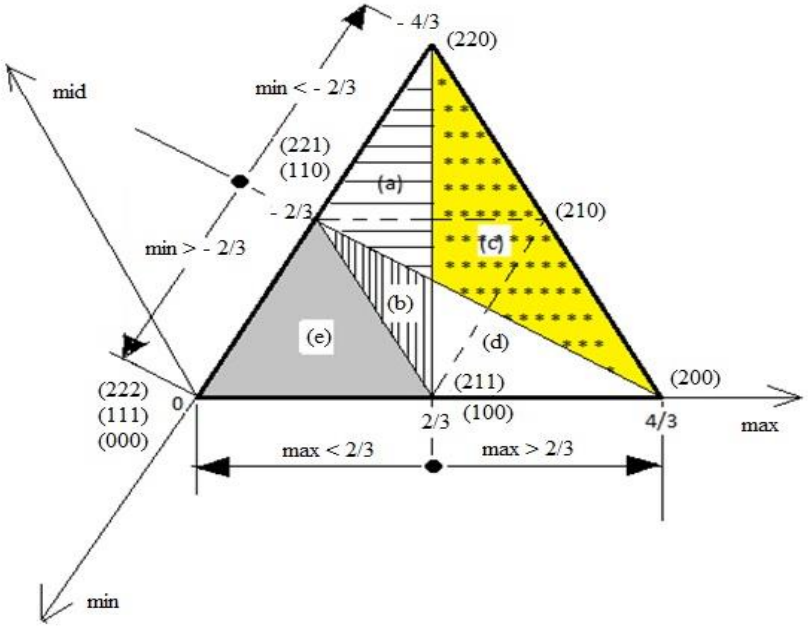


Figure 9. Analysis of the operating regions of the current suppression technique (i_{NP}) for a 3-level NPC inverter in reverse mode.

Adjusting the voltage offset can help control the DC neutral-point current to be different from zero [18]. Its effect is similar to that when we change the duration of action when a phase load is maintained at a certain voltage level; specifically, this involves shifting the d_0 of the max phase to

level 2 and the min phase to level 0. For the mid-phase, this can be achieved by both a d_{01} shift on level 2 and a d_{02} shift on level 0, as shown in Figure 9. The DC neutral-point current iNP at that time is given by:

$$i_{NP} = d_0(i_{\max} - i_{\min}) + \varepsilon i_{mid} \quad (47)$$

In which: $\varepsilon = d_{01} - d_{02}$ and $d_0 = d_{01} + d_{02}$

To control the i_{NP} current, it is necessary to determine the parameters d_0 and ε. From this, the mid-phase displacement range can be determined as follows:

$$\begin{aligned} d_{01} &= (d_0 + \varepsilon)/2 \\ d_{02} &= (d_0 - \varepsilon)/2 \end{aligned} \quad (48)$$

It can be observed that there are two components of the i_{NP} current: one component caused by the change in the voltage offset of the inverter characterized by the quantity d_0, and the other component caused by the asymmetric variation in a mid-phase characterized by the quantity ε. The i_{NP} current controller is based on the mid-phase current. At this point, the simplest method of the three-level technique is to adjust the parameter ε to control the i_{NP} current in accordance with the condition:

$$d_0 = 0,\ \varepsilon \neq 0, \text{ and } i_{NP} = \varepsilon . i_{mid} \quad (49)$$

The magnitude and polarity of the *iNP* current can be controlled based on the following three operating points:

Constraint 1: Corresponding to the *iNP* current being equal to zero:

$$d_0 = \varepsilon = 0;\ d_0 = d_{01} = -d_{20} = \varepsilon = 0$$

Constraint 2: $d_{02} = -d_{01} = d_{1mid}/2$

With this condition, we can deduce:

$$\begin{aligned} \varepsilon &= -d_{1mid} = -[1 - (\max - \min)/2] < 0 \\ i_{NP1} &= -[1 - (\max - \min)/2] i_{mid} \end{aligned} \quad (50)$$

Constraint 3: Based on the relationship between d_{0mid} and d_{2mid}, the i_{NP2} current can attain the following value: $d_{01} = Min(d_{2mid}, d_{0mid})$

(a) $d_{2mid} < d_{0mid}$

$$\begin{aligned} d_{01} &= -d_{02} = d_{2mid}/2 \\ \varepsilon &= d_{2mid} = (mid - \min)/2 > 0 \\ i_{NP2} &= d_{2mid} i_{mid} = (mid - \min)/2 . i_{mid} \end{aligned} \quad (51)$$

(b) $d_{2mid} > d_{0mid}$

$$\begin{aligned} d_{01} &= -d_{02} = d_{0mid}/2 \\ \varepsilon &= d_{0mid} = (\max - mid)/2 > 0 \\ i_{NP2} &= d_{0mid} i_{mid} = (\max - mid)/2 . i_{mid} \end{aligned} \quad (52)$$

From (49) to (52), the *iNP2* current can be either positive or negative. With $i_{mid} > 0$ (or $i_{mid} < 0$), the *iNP* current can be made positive by setting $\varepsilon = d_{0mid}$ or $\varepsilon = d_{2mid}$ (or $\varepsilon = -d_{1mid}$), and negative by setting ($\varepsilon = -d_{1mid}$ $\varepsilon = d_{0mid}$ or $\varepsilon = d_{2mid}$). Similarly, the *iNP* current can be made negative by using analogous reasoning.

3.2. The case of adjusting the *iNP* current based on the max and min phase currents

This approach is suitable when the mid-phase current is small, which makes balancing the DC voltage across the two capacitors inefficient. In this case, the ability to control the *iNP* current based on the maximum and minimum phase currents is a more effective alternative. In this scenario, the control conditions are $d_0 \neq 0$ and ε = 0, resulting in the following outcome:

$$i_{NP} = d_0(i_{\max} - i_{\min}) \quad (53)$$

The two extreme values of the i_{NP} current with opposite polarities correspond to the voltage offsets set as follows:

$$\begin{aligned} d_0 &= d_{0MAX} = Min(d_{2\max}, d_{1\min}, 2d_{2mid}) > 0 \\ d_0 &= d_{0MIN} = -Min(d_{1\max}, d_{0\min}, 2d_{0mid}) < 0 \end{aligned} \quad (54)$$

When selecting, for example, $d_0 = d_{0\max} = d_{2\max}$, the max phase will not switch; similarly, when $d_0 = d_{1\min}$, the min phase will not switch. In the case of $d_0 = 2d_{2mid}$, the mid-phase will operate with a 2-level switching mode [19]. Thus, the control method with a non-zero DC neutral-point current can lead to reduced switching, contributing to lower losses due to switching

compared to the zero DC neutral-point current control method.

4. Simulation and experimental results

Simulation of the 2-level switching, open-loop control. When PF = 0.85, the modulation index increases to 0.8, and the voltage imbalance across the two capacitors is negligible (< 1V) as shown in Figures 9 and 10. Basic simulation parameters:

$V_{c1} = V_{c2} = 200[V]$; $C_1 = C_2 = 68[\mu F]$; R = 5[Ω]; L = 10 [mH]

$f_0 = 50Hz \rightarrow \cos\varphi = 0.85$; $f_{sw} = 5KHz$.

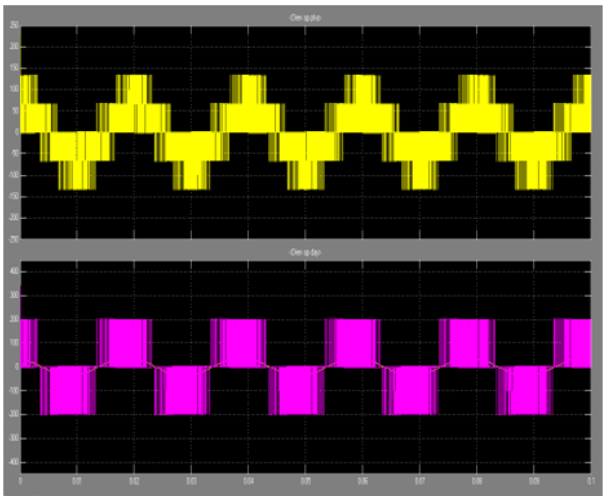


Figure 10. Two-level modulation: Phase voltage and line voltage.

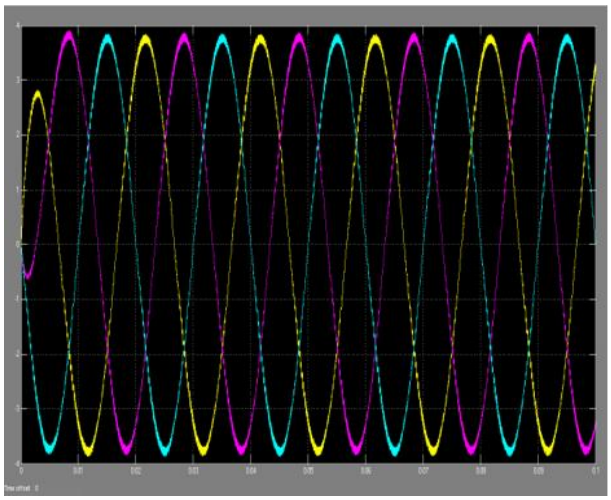
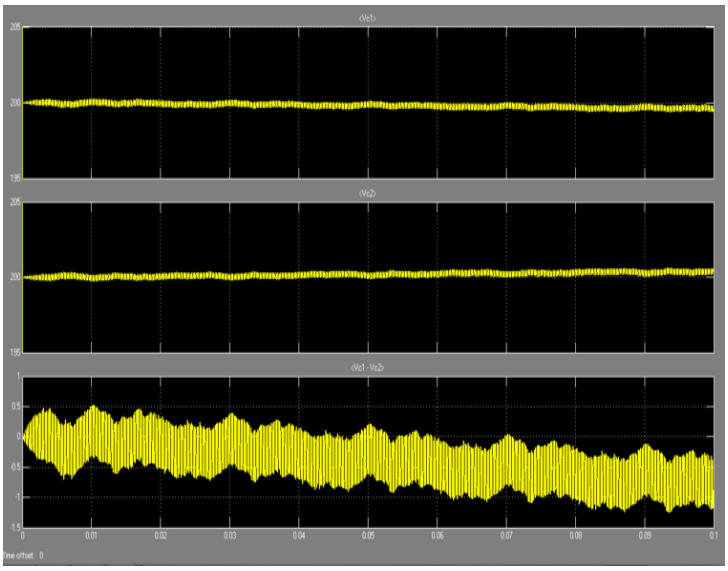


Figure 11. Three-phase load current - Total Harmonic Distortion (THD) = 1.82%.



Figuer 12. Two-level modulation: Voltage across two capacitors Vc1, Vc2, and voltage (Vc1 - Vc2).

Simulation results for the 3-level modulation technique: A three-level NPC inverter is connected to a 3-phase diode rectifier, and the rectified voltage is filtered by two capacitors connected in series. The 3-level modulation technique was applied for two different cases: a) Capacitor C = 2200uF and b) Capacitor C = 68uF. In both cases, the modulation index is set to 0.7, and the voltage across each capacitor is WV = 200V in the balanced state.

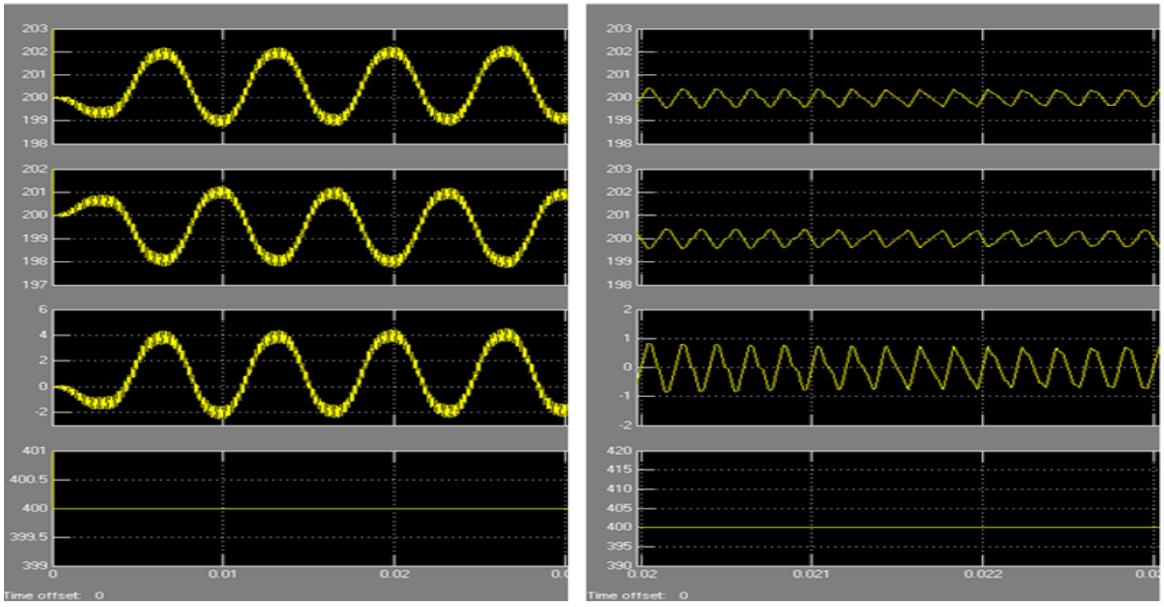


Figure 13. Top to bottom graphs: (a) upper capacitor voltage; (b) lower capacitor voltage; (c) voltage difference between the two capacitors; (d) total voltage for case (1) conventional 2-level modulation (left) and (2) 3-level modulation with zero DC neutral-point current (right).

The following are the experimental results of the 3-level modulation technique with a 2200uF capacitor and RL load.

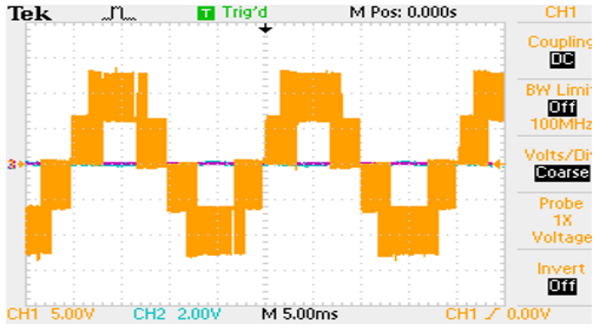


Figure 14. Voltage of the three-level inverter and neutral-point current with no load.

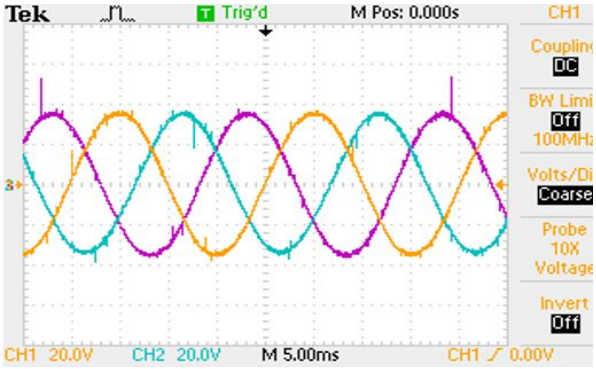


Figure 15. Three-phase current in the case of R-L load.

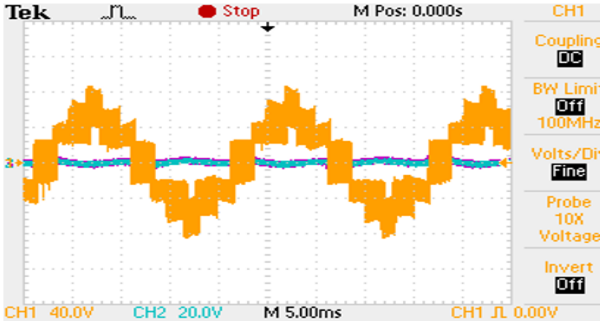


Figure 16. Neutral-point current (i_{NP}) and voltage in the case of an R-L load.

The experimental results described in Figures 14 and 15 demonstrate the ability to effectively maintain the DC neutral-point voltage. The obtained load current had a sinusoidal shape.

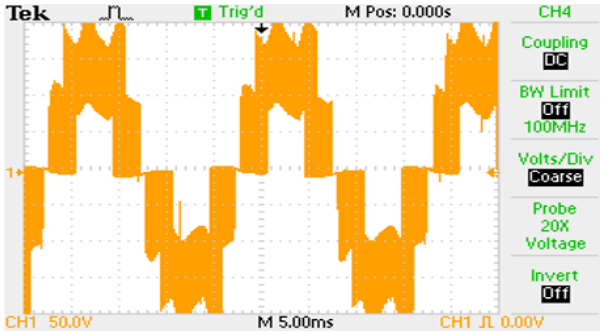


Figure 17. Three-level inverter voltage with R-L load.

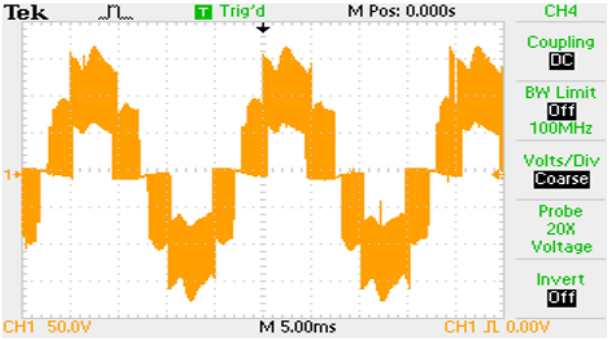


Figure 18. Experimental results with the 3-level modulation technique using a 68uF capacitor and a 3-phase motor load.

5. Conclusion

The initial experimental results demonstrate that the balanced capacitor voltage control algorithm has improved the output quality of the inverter, with a total harmonic distortion (THD) of 1.82%, well within the permissible limits for power ratings ranging from 5 kW to 10 kW [20], [21]. The voltage across each capacitor is maintained at 200 V, and the voltage and current at the neutral point are kept at 0 for both the 2-level and 3-level techniques. Based on these results, the application and utilization of these inverters will lead to improvements in energy efficiency, safety, and overall performance.

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